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	side by side			result set
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<u>L2</u>	L1 same (mode or phase)		25	<u>L2</u>
<u>L1</u>	bridge same "state machine" same (processor or microprocessor or (micro adj1 processor))		170	<u>L1</u>

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<u>L3</u>	L1 same (mode or phase)		0	<u>L3</u>
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
<u>L2</u>	L1 same (mode or phase)		25	<u>L2</u>
<u>L1</u>	bridge same "state machine" same (processor or microprocessor or (micro adj 1 processor))		170	<u>L1</u>

END OF SEARCH HISTORY

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(709/253 712/32 710/306 710/315 710/100 710/313 710/52 710/305 710/5 710/33).ccls.	6948

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Hit Count Set Name

result set

L1 710/306,315,100,313,52,305,5,33;712/32;709/253.ccls. 6948 L1

END OF SEARCH HISTORY

Refine Search

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L1 and L3	33

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DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

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result set

<u>L4</u>	11 and L3	33	<u>L4</u>
<u>L3</u>	(bridge same "state machine") and "real time"	182	<u>L3</u>
<u>L2</u>	bridge same "state machine" same "real time"	3	<u>L2</u>
<u>L1</u>	710/306,315,100,313,52,305,5,33;712/32;709/253.ccls.	6948	<u>L1</u>

END OF SEARCH HISTORY

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Plurals

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Highlight all hit items initially

11 and "real time"

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1	<input type="checkbox"/>	<input type="checkbox"/>	US 6622208	20030916	18	System and methods using a system-on-a-chip	711/118	711/128;
			B2					711/202;
2	<input type="checkbox"/>	<input type="checkbox"/>	US 6362990	20020326	15	Three port content addressable memory device	365/49	365/230.0
			B1					:
3	<input type="checkbox"/>	<input type="checkbox"/>	US 6177808	20010123	10	Integration of bidirectional switches	326/57	326/37;
			B1					326/86
4	<input type="checkbox"/>	<input type="checkbox"/>	US 6163826	20001219	10	Method and apparatus for non-concurrent arbitration	710/107	710/110;
			A					710/240;
5	<input type="checkbox"/>	<input type="checkbox"/>	US 5923859	19990713	35	Dual arbiters for arbitrating access to a	710/113	710/114;
			A					710/119;
6	<input type="checkbox"/>	<input type="checkbox"/>	US 5867728	19990202	12	Preventing corruption in a multiple processor	710/8	710/104
			A					
7	<input type="checkbox"/>	<input type="checkbox"/>	US 5856736	19990105	26	Variable speed AC motor drive for treadmill	318/802	318/811;
			A					482/54
8	<input type="checkbox"/>	<input type="checkbox"/>	US 5828903	19981027	19	System for performing DMA transfer with a pip	710/53	709/212;
			A					710/22
9	<input type="checkbox"/>	<input type="checkbox"/>	US 5797020	19980818	24	Sus master arbitration circuitry having improved	710/240	710/107
			A					
10	<input type="checkbox"/>	<input type="checkbox"/>	US 5793996	19980811	22	Bridge for interconnecting a communication	710/306	345/520;
			A					345/531;
11	<input type="checkbox"/>	<input type="checkbox"/>	US 5747955	19980505	27	Current sensing module	318/434	318/432;

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IEE JNL IEE Journal or Magazine**IEEE CNF** IEEE Conference Proceeding
1. Bridging the gap between formal specification and analysis of communication protocols

Miller, R.E.; Yong Xue;

Computers and Communications, 1996., Conference Proceedings of the 1996 IEEE Fifteenth Annual International Phoenix Conference on
27-29 March 1996 Page(s):225 - 231
Digital Object Identifier 10.1109/PCCC.1996.493638
[AbstractPlus](#) | Full Text: [PDF\(664 KB\)](#) [IEEE CNF](#)

2. Synchronous protocol automata: a framework for modelling and verification of SoC communication architectures

D'silva, V.; Ramesh, S.; Sowmya, A.;

Design, Automation and Test in Europe Conference and Exhibition, 2004. Proceedings
Volume 1, 16-20 Feb. 2004 Page(s):390 - 395 Vol.1
Digital Object Identifier 10.1109/DATE.2004.1268878[AbstractPlus](#) | Full Text: [PDF\(360 KB\)](#) [IEEE CNF](#)

3. One-chip solution in 0.35 /spl mu/m standard CMOS for electronic ballasts for fluorescent lampsKillat, D.; Schmidt, J.; Baumgaertner, A.; Baraniecki, R.; Salzmann, O.;
System-on-Chip, 2003. Proceedings. International Symposium on
19-21 Nov. 2003 Page(s):23 - 26Digital Object Identifier 10.1109/ISSOC.2003.1267708
[AbstractPlus](#) | Full Text: [PDF\(350 KB\)](#) [IEEE CNF](#)

4. Distributed computing with the CLAN networkRiddoch, D.; Mansley, K.; Pope, S.;
Local Computer Networks, 2002. Proceedings. LCN 2002. 27th Annual IEEE Conference on
6-8 Nov. 2002 Page(s):609 - 618[AbstractPlus](#) | Full Text: [PDF\(353 KB\)](#) [IEEE CNF](#)

5. Proceedings of European Design and Test Conference EDAC-ETC-EUROASICEuropean Design and Test Conference, 1994. EDAC, The European Conference on Design Automation. ETC European Test Conference. EUROASIC, The European Event in ASIC Design, Proceedings.
28 Feb.-3 March 1994Digital Object Identifier 10.1109/EDTC.1994.326908
[AbstractPlus](#) | Full Text: [PDF\(16 KB\)](#) [IEEE CNF](#)

6. Bridging the gap between digital circuits and microprocessorsCarpinelli, J.D.; Rosenstark, S.;
Education, IEEE Transactions on
Volume 36, Issue 3, Aug. 1993 Page(s):334 - 339
Digital Object Identifier 10.1109/13.231513

[AbstractPlus](#) | Full Text: [PDF\(472 KB\)](#) IEEE JNL**7. A framework for testing special-purpose memories**

Sidorowicz, P.R.; Brzozowski, J.A.;

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 21, Issue 12, Dec. 2002 Page(s):1459 - 1468
Digital Object Identifier 10.1109/TCAD.2002.804375[AbstractPlus](#) | [References](#) | Full Text: [PDF\(508 KB\)](#) IEEE JNL**8. Synchronous protocol automata: a framework for modelling and verification of SoC communication architectures**

D'silva, V.; Ramesh, S.; Sowmya, A.;

Computers and Digital Techniques, IEE Proceedings-
Volume 152, Issue 1, 14 Jan. 2005 Page(s):20 - 27
Digital Object Identifier 10.1049/ip-cdt:20045097[AbstractPlus](#) | Full Text: [PDF\(537 KB\)](#) IEE JNL**9. Bridge over troubled wrappers: automated interface synthesis**

D'silva, V.; Ramesh, S.; Sowmya, A.;

VLSI Design, 2004. Proceedings. 17th International Conference on
2004 Page(s):189 - 194
Digital Object Identifier 10.1109/ICVD.2004.1260923[AbstractPlus](#) | Full Text: [PDF\(394 KB\)](#) IEEE CND**10. Logician in the land of OS: abstract state machines in Microsoft**

Gurevich, Y.;

Logic in Computer Science, 2001. Proceedings. 16th Annual IEEE Symposium on
16-19 June 2001 Page(s):129 - 136
Digital Object Identifier 10.1109/LICS.2001.932489[AbstractPlus](#) | Full Text: [PDF\(544 KB\)](#) IEEE CND**11. Self test architecture for testing complex memory structures**

Zarrineh, K.; Adams, R.D.; Eckenrode, T.J.; Gregor, S.P.;

Test Conference, 2000. Proceedings. International
3-5 Oct. 2000 Page(s):547 - 556
Digital Object Identifier 10.1109/TEST.2000.894248[AbstractPlus](#) | Full Text: [PDF\(864 KB\)](#) IEEE CND**12. Compiling Verilog into timed finite state machines**

Szu-Tsung Cheng; Brayton, R.K.; York, G.; Yelick, K.; Saldanha, A.;

Verilog HDL Conference, 1995. Proceedings., 1995 IEEE International
27-29 March 1995 Page(s):32 - 39
Digital Object Identifier 10.1109/IVC.1995.512465[AbstractPlus](#) | Full Text: [PDF\(772 KB\)](#) IEEE CND**13. Active objects: a paradigm for communications and event driven systems**

Caal, G.; Divin, A.; Petitpierre, C.;

Global Telecommunications Conference, 1994. GLOBECOM '94. 'Communications: The Global Bridge'., IEEE
28 Nov.-2 Dec. 1994 Page(s):485 - 489 vol.1
Digital Object Identifier 10.1109/GLOCOM.1994.513568[AbstractPlus](#) | Full Text: [PDF\(408 KB\)](#) IEEE CND**14. On testing hierarchies for protocols**

Sidhu, D.P.; Motteler, H.; Vallurupalli, R.;

Networking, IEEE/ACM Transactions on
Volume 1, Issue 5, Oct. 1993 Page(s):590 - 599
Digital Object Identifier 10.1109/90.251917[AbstractPlus](#) | Full Text: [PDF\(1044 KB\)](#) IEEE JNL**15. Scheduling of transactions for system-level test-case generation**

Emek, R.; Naveh, Y.;

High-Level Design Validation and Test Workshop, 2003. Eighth IEEE International

2003 Page(s):149 - 154
Digital Object Identifier 10.1109/HLDVT.2003.1252489

[AbstractPlus](#) | Full Text: [PDF\(477 KB\)](#) [IEEE CNF](#)

 **16. SpecTRM: a CAD system for digital automation**

Leveson, N.G.; Reese, J.D.; Heimdal, M.P.E.;
Digital Avionics Systems Conference, 1998. Proceedings., 17th DASC. The AIAA/IEEE/SAE
Volume 1, 31 Oct.-7 Nov. 1998 Page(s):B52/1 - B52/8 vol.1
Digital Object Identifier 10.1109/DASC.1998.741474

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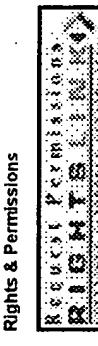


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Dept. of Electr. & Comput. Eng., New Jersey Inst. of Technol., Newark, NJ, USA;

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This paper appears in: **Education, IEEE Transactions on**
 Publication Date: Aug. 1993
 Volume: 36, Issue: 3
 On page(s): 334 - 339
 ISSN: 0018-9359
 CODEN: IEEDAB
 INSPEC Accession Number: 4520712
 Digital Object Identifier: 10.1109/13.231513
 Posted online: 2002-08-06 18:43:53.0

Abstract

Most electrical and computer engineering students understand digital circuits and microprocessors, but fail to appreciate that a microprocessor is just a complex finite state machine. The authors present a three experiment sequence which takes the students from the design of a simple EEPROM-based finite state machine through a two-chip microsequencer to a 4-bit central processing unit (CPU).

Index Terms**Inspec****Controlled Indexing**

EEPROM, computer science education, digital circuits, educational courses, finite state machines, microprocessor chips

Non-controlled Indexing

4-bit, central processing unit, CPU, EEPROM-based finite state machine, complex finite state machine, computer engineering students, digital circuits, electrical engineering students, microprocessor design, microprocessors, microchip, microsequencer

Author Keywords

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References

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L2: Entry 1 of 25

File: PGPB

Mar 17, 2005

PGPUB-DOCUMENT-NUMBER: 20050060479

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20050060479 A1

TITLE: High speed and flexible control for bridge controllers

PUBLICATION-DATE: March 17, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Deng, Brian Tse	Richardson	TX	US	
Nie, Dinghui Richard	Plano	TX	US	
Erickson, Joseph M.	Frisco	TX	US	

APPL-NO: 10/ 651524 [PALM]

DATE FILED: August 29, 2003

INT-CL: [07] G06 E 13/36

US-CL-PUBLISHED: 710/306

US-CL-CURRENT: 710/306

REPRESENTATIVE-FIGURES: 2

ABSTRACT:

A bridge controller controls the data flow to/from a USB bus to/from an ATA/ATAPI drive, such as an ATA hard drive or ATAPI CD or DVD drive. The bridge controller has a state machine which receives the CBW in a background mode in real time as the packet is being transferred to the bridge controller. The state machine uses the CBW to set up the data transfer. The bridge controller also has a programmable processor which is coupled to the CBW once it is received in a buffer memory. The programmable processor makes changes in the set up of the receiving device for the transfer, if needed, and initiates the data transfer.

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File: PGPB

Feb 12, 2004

PGPUB-DOCUMENT-NUMBER: 20040030861

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20040030861 A1

TITLE: Customizable computer system

PUBLICATION-DATE: February 12, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Plackle, Bart	Diest		BE	
Herremans, Kurt	Hasselt		BE	

APPL-NO: 10/ 609141 [PALM]

DATE FILED: June 27, 2003

RELATED-US-APPL-DATA:

Application is a non-provisional-of-provisional application 60/392344, filed June 27, 2002,

INT-CL: [07] G06 F 15/00, G06 F 15/76

US-CL-PUBLISHED: 712/32

US-CL-CURRENT: 712/32

REPRESENTATIVE-FIGURES: 2

ABSTRACT:

A customizable computing system, having a microprocessor and a programmable logic device coupled to the microprocessor via a dedicated bus. The programmable logic device includes a configuration to provide I/O functionality to the system and may be a field programmable gate array. The programmable logic device operates as both a north bridge and a south bridge as is understood by those of ordinary skill in the art. Requests are received from the microprocessor in the programmable logic device over the dedicated bus and are processor specific requests. The processor specific requests are translated into processor dependent commands by a bridge. After the processor specific requests are translated into processor dependent commands, the commands are forwarded to processor independent I/O structures which interface with both internal and external peripheral devices to the customizable computing system.

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This U.S. patent application claims priority from provisional patent application Serial No. 60/392,344 filed on Jun. 27, 2002 entitled "Customizable Computer System" and bearing attorney docket 2684/102 which is incorporated herein by reference in its entirety.

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L2:: Entry 19 of 25

File: USPT

Aug 11, 1998

US-PAT-NO: 5793996

DOCUMENT-IDENTIFIER: US 5793996 A

TITLE: Bridge for interconnecting a computer system bus, an expansion bus and a video frame buffer

DATE-ISSUED: August 11, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Childers; Brian A.	Santa Clara	CA		
Baden; Eric A.	Saratoga	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Apple Computer, Inc.	Cupertino	CA			02

APPL-NO: 08/ 434196 [PALM]

DATE FILED: May 3, 1995

INT-CL: [06] H01 J 13/00

US-CL-ISSUED: 395/309, 395/306, 395/311, 395/307, 395/287, 395/290, 395/851, 395/858, 395/857, 395/847, 395/509, 395/511, 395/512, 395/520, 395/521, 395/526

US-CL-CURRENT: 710/306; 345/520, 345/531, 345/539, 710/107, 710/110, 710/27, 710/31, 710/37, 710/38

FIELD-OF-SEARCH: 395/289, 395/290, 395/287, 395/306, 395/308, 395/311, 395/307, 395/858, 395/476, 395/850, 395/250, 395/281, 395/284, 395/842, 395/847, 395/504, 395/509, 395/511, 395/512

PRIOR-ART-DISCLOSED:

U. S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<u>4935868</u>	June 1990	Dulac	395/308
<u>5255374</u>	October 1993	Aldereguia et al.	395/308
<u>5257348</u>	October 1993	Roskowski et al.	
<u>5257391</u>	October 1993	Dulac et al.	395/800
<u>5263138</u>	November 1993	Wasserman et al.	
<u>5274753</u>	December 1993	Roskowski et al.	
<u>5301272</u>	April 1994	Atkins	

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<input type="checkbox"/>	<u>5553249</u>	September 1996	Datwyler et al.	395/308
<input type="checkbox"/>	<u>5566306</u>	October 1996	Ishida	395/309
<input type="checkbox"/>	<u>5596729</u>	January 1997	Lester et al.	395/308
<input type="checkbox"/>	<u>5606672</u>	February 1997	Wade	395/308
<input type="checkbox"/>	<u>5611058</u>	March 1997	Moore et al.	395/309
<input type="checkbox"/>	<u>5619728</u>	April 1997	Jones et al.	395/847
<input type="checkbox"/>	<u>5621902</u>	April 1997	Cases et al.	395/309
<input type="checkbox"/>	<u>5634013</u>	May 1997	Childers et al.	395/280
<input type="checkbox"/>	<u>5640545</u>	June 1997	Baden et al.	395/515

OTHER PUBLICATIONS

PowerPC 601 RISC Microprocessor User's Manual, pp. 2-42 through 2-70; 8-1 through 8-36; and 9-1 through 9-52, published by Motorola in 1993.

PCI Local Bus Specification, Review Draft Revision 2.1, published Oct. 21, 1994 by the PCI Special Interest Group, P.O. Box 14070, Portland, OR 97214.

PCI Multimedia Design Guide, Revision 1.0 (Mar. 29, 1994), which is distributed by the PCI Multimedia Working Group (part of the PCI Special Interest Group, P.O. Box 14070, Portland, OR 97214).

ART-UNIT: 235

PRIMARY-EXAMINER: Harvey; Jack B.

ASSISTANT-EXAMINER: Phan; Raymond N.

ATTY-AGENT-FIRM: Burns, Doane, Swecker & Mathis, LLP

ABSTRACT:

In a computer system an apparatus interconnects a first bus, a second bus and a frame buffer, wherein the first bus and the second bus are of incompatible bus architecture types. For example the first bus may be a loosely coupled bus having split-bus transaction capability, such as the ARBus, and the second bus may be a tightly ordered bus, such as the PCI local bus. The apparatus includes bridge hardware for converting access requests from the first bus into suitable requests for the second bus. Data paths within the apparatus allow data to be routed from one bus to another. The apparatus further includes a frame buffer controller that is accessible from either of the first or second buses for performing read or write operations from/to the frame buffer. Data path logic allows data to be routed from any of the first bus, second bus and frame buffer to any other one of these three locations. In a preferred embodiment, the data paths are fabricated on a first integrated circuit, and all of control logic is fabricated on a second integrated circuit. The partitioning of hardware in this manner allows for an efficient interface to be provided between the two chips.

12 Claims, 12 Drawing figures

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L2: Entry 19 of 25

File: USPT

Aug 11, 1998

US-PAT-NO: 5793996

DOCUMENT-IDENTIFIER: US 5793996 A

TITLE: Bridge for interconnecting a computer system bus, an expansion bus and a video frame buffer

DATE-ISSUED: August 11, 1998**INVENTOR-INFORMATION:**

NAME	CITY	STATE	ZIP CODE	COUNTRY
Childers; Brian A.	Santa Clara	CA		
Baden; Eric A.	Saratoga	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Apple Computer, Inc.	Cupertino	CA			02

APPL-NO: 08/ 434196 [PALM]

DATE FILED: May 3, 1995

INT-CL: [06] H01 J 13/00

US-CL-ISSUED: 395/309, 395/306, 395/311, 395/307, 395/287, 395/290, 395/851, 395/858, 395/857, 395/847, 395/509, 395/511, 395/512, 395/520, 395/521, 395/526

US-CL-CURRENT: 710/306; 345/520, 345/531, 345/539, 710/107, 710/110, 710/27, 710/31, 710/37, 710/38

FIELD-OF-SEARCH: 395/289, 395/290, 395/287, 395/306, 395/308, 395/311, 395/307, 395/858, 395/476, 395/850, 395/250, 395/281, 395/284, 395/842, 395/847, 395/504, 395/509, 395/511, 395/512

PRIOR-ART-DISCLOSED:

U. S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<u>4935868</u>	June 1990	Dulac	395/308
<u>5255374</u>	October 1993	Aldereguia et al.	395/308
<u>5257348</u>	October 1993	Roskowski et al.	
<u>5257391</u>	October 1993	Dulac et al.	395/800
<u>5263138</u>	November 1993	Wasserman et al.	
<u>5274753</u>	December 1993	Roskowski et al.	
<u>5301272</u>	April 1994	Atkins	

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<input type="checkbox"/>	<u>5596729</u>	January 1997	Lester et al.	395/308
<input type="checkbox"/>	<u>5606672</u>	February 1997	Wade	395/308
<input type="checkbox"/>	<u>5611058</u>	March 1997	Moore et al.	395/309
<input type="checkbox"/>	<u>5619728</u>	April 1997	Jones et al.	395/847
<input type="checkbox"/>	<u>5621902</u>	April 1997	Cases et al.	395/309
<input type="checkbox"/>	<u>5634013</u>	May 1997	Childers et al.	395/280
<input type="checkbox"/>	<u>5640545</u>	June 1997	Baden et al.	395/515

OTHER PUBLICATIONS

PowerPC 601 RISC Microprocessor User's Manual, pp. 2-42 through 2-70; 8-1 through 8-36; and 9-1 through 9-52, published by Motorola in 1993.

PCI Local Bus Specification, Review Draft Revision 2.1, published Oct. 21, 1994 by the PCI Special Interest Group, P.O. Box 14070, Portland, OR 97214.

PCI Multimedia Design Guide, Revision 1.0 (Mar. 29, 1994), which is distributed by the PCI Multimedia Working Group (part of the PCI Special Interest Group, P.O. Box 14070, Portland, OR 97214).

ART-UNIT: 235

PRIMARY-EXAMINER: Harvey; Jack B.

ASSISTANT-EXAMINER: Phan; Raymond N.

ATTY-AGENT-FIRM: Burns, Doane, Swecker & Mathis, LLP

ABSTRACT:

In a computer system an apparatus interconnects a first bus, a second bus and a frame buffer, wherein the first bus and the second bus are of incompatible bus architecture types. For example the first bus may be a loosely coupled bus having split-bus transaction capability, such as the ARBus, and the second bus may be a tightly ordered bus, such as the PCI local bus. The apparatus includes bridge hardware for converting access requests from the first bus into suitable requests for the second bus. Data paths within the apparatus allow data to be routed from one bus to another. The apparatus further includes a frame buffer controller that is accessible from either of the first or second buses for performing read or write operations from/to the frame buffer. Data path logic allows data to be routed from any of the first bus, second bus and frame buffer to any other one of these three locations. In a preferred embodiment, the data paths are fabricated on a first integrated circuit, and all of control logic is fabricated on a second integrated circuit. The partitioning of hardware in this manner allows for an efficient interface to be provided between the two chips.

12 Claims, 12 Drawing figures

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L2: Entry 19 of 25

File: USPT

Aug 11, 1998

US-PAT-NO: 5793996

DOCUMENT-IDENTIFIER: US 5793996 A

TITLE: Bridge for interconnecting a computer system bus, an expansion bus and a video frame buffer

DATE-ISSUED: August 11, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Childers; Brian A.	Santa Clara	CA		
Baden; Eric A.	Saratoga	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Apple Computer, Inc.	Cupertino	CA			02

APPL-NO: 08/ 434196 [PALM]

DATE FILED: May 3, 1995

INT-CL: [06] H01 J 13/00

US-CL-ISSUED: 395/309, 395/306, 395/311, 395/307, 395/287, 395/290, 395/851, 395/858, 395/857, 395/847, 395/509, 395/511, 395/512, 395/520, 395/521, 395/526

US-CL-CURRENT: 710/306; 345/520, 345/531, 345/539, 710/107, 710/110, 710/27, 710/31, 710/37, 710/38

FIELD-OF-SEARCH: 395/289, 395/290, 395/287, 395/306, 395/308, 395/311, 395/307, 395/858, 395/476, 395/850, 395/250, 395/281, 395/284, 395/842, 395/847, 395/504, 395/509, 395/511, 395/512

PRIOR-ART-DISCLOSED:

U. S. PATENT DOCUMENTS

 [Search Selected](#) [Search All](#) [Clear](#)

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<u>4935868</u>	June 1990	Dulac	395/308
<u>5255374</u>	October 1993	Aldereguia et al.	395/308
<u>5257348</u>	October 1993	Roskowski et al.	
<u>5257391</u>	October 1993	Dulac et al.	395/800
<u>5263138</u>	November 1993	Wasserman et al.	
<u>5274753</u>	December 1993	Roskowski et al.	
<u>5301272</u>	April 1994	Atkins	

<input type="checkbox"/>	<u>5359715</u>	October 1994	Heil et al.	395/308
<input type="checkbox"/>	<u>5488695</u>	January 1996	Cutter	395/290
<input type="checkbox"/>	<u>5544334</u>	August 1996	Noll	395/309
<input type="checkbox"/>	<u>5553249</u>	September 1996	Datwyler et al.	395/308
<input type="checkbox"/>	<u>5566306</u>	October 1996	Ishida	395/309
<input type="checkbox"/>	<u>5596729</u>	January 1997	Lester et al.	395/308
<input type="checkbox"/>	<u>5606672</u>	February 1997	Wade	395/308
<input type="checkbox"/>	<u>5611058</u>	March 1997	Moore et al.	395/309
<input type="checkbox"/>	<u>5619728</u>	April 1997	Jones et al.	395/847
<input type="checkbox"/>	<u>5621902</u>	April 1997	Cases et al.	395/309
<input type="checkbox"/>	<u>5634013</u>	May 1997	Childers et al.	395/280
<input type="checkbox"/>	<u>5640545</u>	June 1997	Baden et al.	395/515

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PCI Multimedia Design Guide, Revision 1.0 (Mar. 29, 1994), which is distributed by the PCI Multimedia Working Group (part of the PCI Special Interest Group, P.O. Box 14070, Portland, OR 97214).

ART-UNIT: 235

PRIMARY-EXAMINER: Harvey; Jack B.

ASSISTANT-EXAMINER: Phan; Raymond N.

ATTY-AGENT-FIRM: Burns, Doane, Swecker & Mathis, LLP

ABSTRACT:

In a computer system an apparatus interconnects a first bus, a second bus and a frame buffer, wherein the first bus and the second bus are of incompatible bus architecture types. For example the first bus may be a loosely coupled bus having split-bus transaction capability, such as the ARBus, and the second bus may be a tightly ordered bus, such as the PCI local bus. The apparatus includes bridge hardware for converting access requests from the first bus into suitable requests for the second bus. Data paths within the apparatus allow data to be routed from one bus to another. The apparatus further includes a frame buffer controller that is accessible from either of the first or second buses for performing read or write operations from/to the frame buffer. Data path logic allows data to be routed from any of the first bus, second bus and frame buffer to any other one of these three locations. In a preferred embodiment, the data paths are fabricated on a first integrated circuit, and all of control logic is fabricated on a second integrated circuit. The partitioning of hardware in this manner allows for an efficient interface to be provided between the two chips.

12 Claims, 12 Drawing figures

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L2: Entry 23 of 25

File: USPT

Oct 22, 1996

US-PAT-NO: 5568613

DOCUMENT-IDENTIFIER: US 5568613 A

TITLE: Dataframe bridge filter with communication node recordkeeping

DATE-ISSUED: October 22, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Futral; William T.	Hillsboro	OR		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Ungermann-Bass, Inc.	Santa Clara	CA			02

APPL-NO: 07/ 939777 [PALM]

DATE FILED: September 3, 1992

INT-CL: [06] G06 F 13/00, G06 F 13/14, G06 F 12/06

US-CL-ISSUED: 395/200.02, 395/200.11, 395/835, 395/839, 364/246, 364/246.12, 364/246.3

US-CL-CURRENT: 709/249; 710/15, 710/19

FIELD-OF-SEARCH: 395/200, 395/800, 395/325, 395/400, 395/200.02, 395/200.11, 395/835, 395/839, 370/94.1

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<u>4737953</u>	April 1988	Koch et al.	370/94
<u>4811203</u>	March 1989	Hamstra	364/200
<u>4853921</u>	August 1989	Takeda	369/59
<u>4922503</u>	May 1990	Leone	370/85.13
<u>4926420</u>	May 1990	Shimizu	370/94.1
<u>4967353</u>	October 1990	Brenner et al.	364/200
<u>5125085</u>	June 1992	Phillips	395/400
<u>5136580</u>	August 1992	Videlock et al.	370/60
<u>5245606</u>	September 1993	DeSouza	370/85.13
<u>5321695</u>	June 1994	Faulk, Jr.	370/94.1

ART-UNIT: 237

PRIMARY-EXAMINER: Lee; Thomas C.

ASSISTANT-EXAMINER: Krick; Rehana

ATTY-AGENT-FIRM: Townsend and Townsend and Crew

ABSTRACT:

A dataframe filter is provided a local area network bridge to monitor the dataframes transmitted on one network to determine those dataframes destined to be communicated to another network by the network bridge. The filter receives and examines the destination address of each dataframe communicated on the one filter and, searching through a database maintained by the filter, determine whether the destination address is located on the second network and, if so, signals the bridge to copy the dataframe to the second network.

10 Claims, 6 Drawing figures

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L2: Entry 23 of 25

File: USPT

Oct 22, 1996

US-PAT-NO: 5568613

DOCUMENT-IDENTIFIER: US 5568613 A

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DATE-ISSUED: October 22, 1996

INVENTOR-INFORMATION:

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DATE FILED: September 3, 1992

INT-CL: [06] G06 F 13/00, G06 F 13/14, G06 F 12/06

US-CL-ISSUED: 395/200.02; 395/200.11, 395/835, 395/839, 364/246, 364/246.12, 364/246.3

US-CL-CURRENT: 709/249; 710/15, 710/19

FIELD-OF-SEARCH: 395/200, 395/800, 395/325, 395/400, 395/200.02, 395/200.11, 395/835, 395/839, 370/94.1

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/> <u>4737953</u>	April 1988	Koch et al.	370/94
<input type="checkbox"/> <u>4811203</u>	March 1989	Hamstra	364/200
<input type="checkbox"/> <u>4853921</u>	August 1989	Takeda	369/59
<input type="checkbox"/> <u>4922503</u>	May 1990	Leone	370/85.13
<input type="checkbox"/> <u>4926420</u>	May 1990	Shimizu	370/94.1
<input type="checkbox"/> <u>4967353</u>	October 1990	Brenner et al.	364/200
<input type="checkbox"/> <u>5125085</u>	June 1992	Phillips	395/400
<input type="checkbox"/> <u>5136580</u>	August 1992	Videlock et al.	370/60
<input type="checkbox"/> <u>5245606</u>	September 1993	DeSouza	370/85.13
<input type="checkbox"/> <u>5321695</u>	June 1994	Faulk, Jr.	370/94.1

ART-UNIT: 237

PRIMARY-EXAMINER: Lee; Thomas C.

ASSISTANT-EXAMINER: Krick; Rehana

ATTY-AGENT-FIRM: Townsend and Townsend and Crew

ABSTRACT:

A dataframe filter is provided a local area network bridge to monitor the dataframes transmitted on one network to determine those dataframes destined to be communicated to another network by the network bridge. The filter receives and examines the destination address of each dataframe communicated on the one filter and, searching through a database maintained by the filter, determine whether the destination address is located on the second network and, if so, signals the bridge to copy the dataframe to the second network.

10 Claims, 6 Drawing figures

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US5923859A
United States Patent

(19)

Melo et al.

(11) Patent Number: 5,923,859

(45) Date of Patent: Jul 13, 1999

(54) DUAL ARBITERS FOR ARBITRATING ACCESS TO A FIRST AND SECOND BUS IN A COMPUTER SYSTEM HAVING BUS MASTERS ON EACH BUS

5,724,231 6/1998 Linck et al. 375,476
5,728,760 4/1998 Ziegler et al. 375,233
5,731,992 7/1998 Tisay et al. 375,003
5,756,779 1/1998 Leder et al. 375,008

(75) Inventor: Mark L. Melo, Robert Allen Lester,
5011 of Houston, Tex.

FOREIGN PATENT DOCUMENTS

(73) Assignee: Compaq Computer Corporation,
Houston, Tex.

6344214 6/1999 Doherty, Jr., et al.

OTHER PUBLICATIONS

(21) Appl. No.: 08/974,149

623,762B PCI-EISA Bridge (PCB) Order No. 200-
220477-001, Apr. 1993.

(22) Filed: Nov. 18, 1997

574,203/524,430 PCI SEL, ISA and EISA Bridges, Intel Corp.,
pp. 1-3, 17, 35, 37, 48, 154-157, 173-174, 211, 221-226,
243-252, 310-321, 345, 343-354, 438-441, 442-462
(1993).

Related U.S. Application Data

Proprietary Components, Intel Corp., pp. 1-215, 1-222 to
1-223, 1-241 to 1-245, 1-245 to 1-267, 1-263 to 1-264
(1993).Continuation of application No. 08/427,202, Apr. 13, 1995,
abandoned.Priority Examiner—Atta R. Shokouh
Assistant Examiner—Eric S. Tolson
Attorney, Agent or Firm—Adrian Comp, San Jose, Calif.
Pixel, L.L.P.

(58) Field of Search 395,732, 294,

(57) ABSTRACT

395,733, 294, 395,725,

395,728, 395,729

395,730, 395,731, 395,732

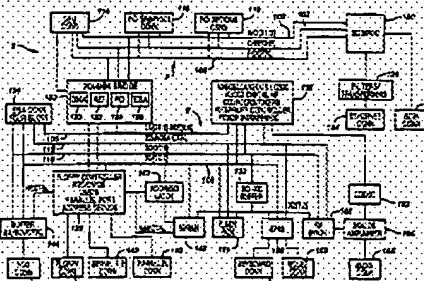
395,733, 726, 729

References Cited

U.S. PATENT DOCUMENTS

4,751,938 7/1988 Ishizaki et al.
4,983,854 12/1990 Dravidian et al.
5,007,220 3/1991 Croft et al. 364,200
5,008,285 3/1991 Takemoto et al.
5,151,934 9/1992 Weller et al.
5,191,656 3/1993 Fecio, III et al.
5,212,785 5/1993 Allison
5,301,382 4/1994 Austin et al. 395,725
5,311,276 5/1994 Hellerstedt
5,333,276 7/1994 Austin et al. 395,725
5,338,655 8/1994 Croft et al. 395,725
5,446,742 8/1995 Bannister et al. 395,725

12 Claims, 18 Drawing Sheets



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L4: Entry 11 of 33

File: USPT

Sep 7, 2004

US-PAT-NO: 6789153

DOCUMENT-IDENTIFIER: US 6789153 B1

TITLE: Bridge for coupling digital signal processor to on-chip bus as slave

DATE-ISSUED: September 7, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Stewart; Charles H.	Richardson	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
LSI Logic Corporation	Milpitas	CA			02

APPL-NO: 09/ 847850 [PALM]

DATE FILED: April 30, 2001

PARENT-CASE:

CROSS-REFERENCE TO RELATED APPLICATIONS This application claims priority based on provisional patent application Serial No. 60/270,063, filed Feb. 20, 2001. This application incorporates by reference for all purposes, the following applications, filed on the same date as this application and assigned to the same assignee as the present application: U.S. patent application Ser. No. 09/847,850, filed Apr. 30, 2001, now U.S. Pat. No. 6,687,773, issued Feb. 3, 2004, entitled "Bridge For Coupling Digital Signal Processor to AMBA Bus as Master" by inventors Charles H. Stewart and Keith D. Dang; and U.S. patent application Ser. No. 09/847,848, filed Apr. 30, 2001, entitled "A Parameterizable Queued Memory Access System" by inventor Charles H. Stewart.

INT-CL: [07] G06 F 13/00

US-CL-ISSUED: 710/306; 710/65, 710/311, 710/315

US-CL-CURRENT: 710/306; 710/311, 710/315, 710/65

FIELD-OF-SEARCH: 710/65, 710/306-315

PRIOR-ART-DISCLOSED:

U. S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<u>6128673</u>	October 2000	Aronson et al.	
<u>6247082</u>	June 2001	Lo et al.	710/105
<u>6467010</u>	October 2002	Pontius et al.	710/305
<u>6529847</u>	March 2003	Hamilton et al.	

<input type="checkbox"/>	<u>6567881</u>	May 2003	Mojaver et al.	710/313
<input type="checkbox"/>	<u>6571308</u>	May 2003	Reiss et al.	
<input type="checkbox"/>	<u>6604163</u>	August 2003	Duboc	710/306
<input type="checkbox"/>	<u>6654844</u>	November 2003	Piirainen et al.	710/305
<input type="checkbox"/>	<u>2001/0016885</u>	August 2001	Happonen	710/52

ART-UNIT: 2112

PRIMARY-EXAMINER: Auve; Glenn A.

ASSISTANT-EXAMINER: Patel; Nimesh

ATTY-AGENT-FIRM: Conley, Rose P.C.

ABSTRACT:

A bridge for connecting a DSP to an ASIC on-chip bus as a slave. The bridge couples signals between a DSP internal memory direct memory interface and an on-chip bus such as the AMBA AHB. The bridge includes a generic slave module which provides direct connections to the on-chip bus in the on-chip bus protocol. It also includes a slave engine connected to the DSP memory interface to control read and write transactions with the memory. The generic slave and the slave engine are coupled by a pulse grower and pulse shaver to allow the engine to operate at DSP clock frequency while the generic slave operates at the usually slower on-chip bus frequency. The bridge allows masters in the ASIC to perform read and write transactions with the DSP internal memory.

27 Claims, 12 Drawing figures

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L4: Entry 29 of 33

File: USPT

Aug 11, 1998

US-PAT-NO: 5793996

DOCUMENT-IDENTIFIER: US 5793996 A

TITLE: Bridge for interconnecting a computer system bus, an expansion bus and a video frame buffer

DATE-ISSUED: August 11, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Childers; Brian A.	Santa Clara	CA		
Baden; Eric A.	Saratoga	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Apple Computer, Inc.	Cupertino	CA			02

APPL-NO: 08/ 434196 [PALM]

DATE FILED: May 3, 1995

INT-CL: [06] H01 J 13/00

US-CL-ISSUED: 395/309, 395/306, 395/311, 395/307, 395/287, 395/290, 395/851, 395/858, 395/857, 395/847, 395/509, 395/511, 395/512, 395/520, 395/521, 395/526

US-CL-CURRENT: 710/306; 345/520, 345/531, 345/539, 710/107, 710/110, 710/27, 710/31, 710/37, 710/38

FIELD-OF-SEARCH: 395/289, 395/290, 395/287, 395/306, 395/308, 395/311, 395/307, 395/858, 395/476, 395/850, 395/250, 395/281, 395/284, 395/842, 395/847, 395/504, 395/509, 395/511, 395/512

PRIOR-ART-DISCLOSED:

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<input type="checkbox"/>	<u>5596729</u>	January 1997	Lester et al.	395/308
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<input type="checkbox"/>	<u>5611058</u>	March 1997	Moore et al.	395/309
<input type="checkbox"/>	<u>5619728</u>	April 1997	Jones et al.	395/847
<input type="checkbox"/>	<u>5621902</u>	April 1997	Cases et al.	395/309
<input type="checkbox"/>	<u>5634013</u>	May 1997	Childers et al.	395/280
<input type="checkbox"/>	<u>5640545</u>	June 1997	Baden et al.	395/515

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PCI Local Bus Specification, Review Draft Revision 2.1, published Oct. 21, 1994 by the PCI Special Interest Group, P.O. Box 14070, Portland, OR 97214.

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ART-UNIT: 235

PRIMARY-EXAMINER: Harvey; Jack B.

ASSISTANT-EXAMINER: Phan; Raymond N.

ATTY-AGENT-FIRM: Burns, Doane, Swecker & Mathis, LLP

ABSTRACT:

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12 Claims, 12 Drawing figures

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